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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,360	04/28/2006	Masaru Takaishi	AI 411NP	5184

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EXAMINER	
HO, HOANG QUAN TRAN	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
02/05/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,360	TAKAISHI, MASARU	
	Examiner	Art Unit	
	Hoang-Quan T. Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *4,10,14 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-13,15-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/28/06,9/4/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species I in the reply filed on October 21, 2008 is acknowledged.

Claims 4, 10, 14, and 18 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species II – III, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 21, 2008.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on April 28, 2006 and September 4, 2008 are being considered by the examiner.

Drawings

Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 3, 5 – 9, 11 – 13, 15 – 17, and 19 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitoh et al. (U.S. Pat. App. Pub. No. 2002/0185705 A1), hereinafter as Saitoh, and further in view of Saito et al. (U.S. Pat. App. Pub. No. 2002/0005549 A1), hereinafter as Saito.

Regarding claim 1, figs. 8 and 10A and ¶169 of Saitoh discloses a production method for a semiconductor device which includes a super junction structural portion (refs. 18 – 19) provided on a semiconductor substrate (ref. 11) of a first conductivity (n type as seen in fig. 8) and including drift layers (ref. 19) of the first conductivity (n type as seen in fig. 8) and RESURF layers (ref. 18) of a second conductivity (p type as seen in fig. 8) different from the first conductivity (p type vs. n type as seen in fig. 8), the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate (as seen in fig. 8), the production method comprising the steps of:

forming a semiconductor layer (ref. 19) of the first conductivity (n type as seen in fig. 8) on the semiconductor substrate (as seen in fig. 7A);

forming a trench (ref. 24) in the semiconductor layer, the trench penetrating through the semiconductor layer to reach the semiconductor substrate (as seen in fig. 7B);

filling a filling material (ref. 22) in a predetermined bottom portion of the trench (as seen in fig. 7E).

Saitoh may not disclose the following limitations whereas figs. 13 – 14G of Saito disclose that it is known in the art to provide:

so that a filling material (ref. 8b) portion is provided in the bottom portion of the trench (ref. 32) up to a predetermined upper surface position which is shallower than an interface between the semiconductor substrate and the semiconductor layer (¶137 – 140 discloses that ref. 18b are created within the drift layer, therefore, one of ordinary

skill in the art would be capable of providing ref. 18b at substantially the same depth as an interface between the isolation region and the RESURF layer, to provide charge trapping and improving breakdown voltage; also see ¶198 where it discloses buried layers in a drift layer are equivalent of RESURF layers, therefore the combination provides the benefits of improving breakdown voltage) and a void is provided in an upper portion of the trench above the predetermined upper surface position (as seen in fig. 14F); and

after the filling step (in view of MPEP § 2144.04(IV)(C), selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results), introducing an impurity of the second conductivity into a portion of the semiconductor layer exposed to an interior side wall of the trench (as seen in fig. 7C of Saitoh), whereby the RESURF layers of the second conductivity are each formed alongside the interior side wall of the trench and the drift layers are each defined by a portion of the semiconductor layer remaining intact (as seen in fig. 7E of Saitoh).

Regarding claim 2, Saitoh and Saito disclose a semiconductor device production method as set forth in claim 1, figs. 14A – 14G of Saito discloses wherein the filling step includes the steps of:

supplying the filling material (ref. 34a) into the trench (ref. 32) up to a position which is shallower than the predetermined upper surface position (¶137 – 140 discloses that ref. 18b are created within the drift layer, therefore, one of ordinary skill in the art would be capable of providing ref. 18b at substantially the same depth as an interface

between the isolation region and the RESURF layer, to provide charge trapping and improving breakdown voltage; also see ¶198 where it discloses buried layers in a drift layer are equivalent of RESURF layers, therefore the combination provides the benefits of improving breakdown voltage); and

after the filling material supplying step, etching back the supplied filling material to the predetermined upper surface position (as seen in fig. 14D; ¶142).

Regarding claims 3 and 13, Saitoh and Saito disclose a semiconductor device production method as set forth in claims 1 and 2, Saitoh and Saito disclose wherein the filling step includes the step of filling silicon oxide as the filling material in the trench (¶167 of Saitoh discloses that it is an insulating layer, however ¶346 of Saitoh discloses that it is known to provide a silicon oxide as the insulation layer material; ¶139 of Saito).

Regarding claims 5 and 15, Saitoh and Saito disclose a semiconductor device production method as set forth in claims 1 and 2, ¶144 of Saito discloses further comprising the step of filling the void provided in the upper portion of the trench with an upper filling material (ref. 34c) after the RESURF layer formation step (in view of MPEP § 2144.04(IV)(C), selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results).

Regarding claims 6 and 16, Saitoh and Saito disclose a semiconductor device production method as set forth in claims 1 and 2, Saitoh discloses further comprising the steps of:

introducing an impurity of the second conductivity (p type as seen in fig. 8) into a surface portion of the semiconductor layer to form a base region (ref. 12) of the second conductivity (p type as seen in fig. 8) in contact with the RESURF layer and the drift layer (as seen in fig. 8);

introducing an impurity of the first conductivity (n type as seen in fig. 8) into a portion of the base region to form a source region (ref. 13) of the first conductivity (n type as seen in fig. 8) which is isolated from the drift layer and the RESURF layer by the other portion of the base region (as seen in fig. 8);

forming a gate insulation film (ref. 14) opposed to a portion of the base region between the source region and the drift layer (as seen in fig. 8); and

forming a gate electrode (ref. 15) opposed to the portion of the base region between the source region and the drift layer with the intervention of the gate insulation film (as seen in fig. 8).

Regarding claims 7 and 17, Saitoh and Saito disclose a semiconductor device production method as set forth in claims 1 and 2, Saitoh discloses wherein the RESURF layer formation step includes the steps of:

implanting the impurity of the second conductivity into a surface portion of the semiconductor layer exposed to the interior side wall of the trench (¶159 and fig. 7C); and

performing a thermal diffusion process to heat the resulting semiconductor substrate after the implantation step for diffusing the implanted impurity into the semiconductor layer (¶160).

Regarding claim 8, figs. 8 and 10A of Saitoh discloses a semiconductor device, comprising:

a semiconductor substrate (ref. 11) of a first conductivity (n type as seen in fig. 8);

a super junction structural portion (refs. 18 – 19) provided on the semiconductor substrate (as seen in fig. 8) and including drift layers (ref. 19) of the first conductivity (n type as seen in fig. 8) and RESURF layers (ref. 18) of a second conductivity (p type as seen in fig. 8) different from the first conductivity (p type vs. n type as seen in fig. 8), the drift layers and the RESURF layers being laterally arranged in alternate relation in a direction parallel to the semiconductor substrate (as seen in fig. 8); and

filling material portions (ref. 22) each provided in a predetermined bottom portion of a trench (e.g., ref. 24 of fig. 7B; i.e., ref. 22 is provided in a trench) penetrating through the super junction structural portion to reach the semiconductor substrate (as seen in fig. 8), wherein

the RESURF layers are each provided alongside an interior side wall of the trench (as seen in fig. 8), the drift layers each have an isolation region (ref. 11d) present between the RESURF layer and the semiconductor substrate to prevent the RESURF layer from contacting the semiconductor substrate (as seen in fig. 10A; ¶176 – 181 discloses an advantage of a depletion layer hardly spreading to the isolation region).

Saitoh may not disclose the following limitations whereas fig. 13 of Saito discloses that it is known in the art to provide:

the filling material portions (ref. 8b) each have an upper surface (where ref. 8b meets ref. 18b) located at substantially the same depth as an interface between the isolation region and the RESURF layer as measured from a surface of the super junction structural portion (¶137 – 140 discloses that ref. 18b are created within the drift layer, therefore, one of ordinary skill in the art would be capable of providing ref. 18b at substantially the same depth as an interface between the isolation region and the RESURF layer, to provide charge trapping and improving breakdown voltage; also see ¶198 where it discloses buried layers in a drift layer are equivalent of RESURF layers, therefore the combination provides the benefits of improving breakdown voltage).

Regarding claim 9, Saitoh and Saito disclose a semiconductor device as set forth in claim 8, Saitoh and Saito disclose wherein the filling material portions each comprise a silicon oxide portion (¶167 of Saitoh discloses that it is an insulating layer, however ¶346 of Saitoh discloses that it is known to provide a silicon oxide as the insulation layer

material; ¶139 of Saito).

Regarding claims 11 and 19, Saitoh and Saito disclose a semiconductor device as set forth in claims 8 and 9, Saito discloses further comprising upper filling material portions (ref. 8b as seen in fig. 13) each provided in an upper portion of the trench above the filling material portion (i.e., a lower ref. 8b as opposed to an upper portion of ref. 8b as seen in fig. 13).

Regarding claims 12 and 20, Saitoh and Saito disclose a semiconductor device as set forth in claims 8 and 9, Saitoh disclose further comprising:

base regions (ref. 12) of the second conductivity (p type as seen in fig. 8) each provided in contact with the drift layer and the RESURF layer (as seen in fig. 8);

source regions (ref. 13) of the first conductivity (n type as seen in fig. 8) each provided in contact with the base region and isolated from the drift layer and the RESURF layer by the base region (as seen in fig. 8); and

gate electrodes (ref. 15) each provided in opposed relation to a portion of the base region between the source region and the drift layer (as seen in fig. 8) with the intervention of a gate insulation film (ref. 14).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan T. Ho whose telephone number is 571-272-8711. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoang-Quan T Ho/
Examiner, Art Unit 2818
February 2, 2009

/Andy Huynh/
Primary Examiner, Art Unit 2818